GA-M68M-S2P

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03	BLOCK DIAGRAM
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21	Realtek 8211 CL
22	H/W MONITOR & FAN CONTROL
23	IDE,FDD,COM,LPT
24	F_USB, R_USB
25	ALC888B HD-AUDIO

P-Code:U96133-0

SHEET	TITLE
26	AUDIO JACK, L_OUT, F_AUDIO
27	ATX, VCC12_DUAL, VDDA25 F_PANEL POWER SEQ
28	PWM ISL6324

Revision

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<OrgAddr1>

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M68M-S2P | Rev: 2.3

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Model Name:GA-M68M-S2P Rev.2.3

Component value change history

P-Code: U96133-0

Date	Change Item		Reason
2009.08.05	1.0A E_BOM issue	PCB:1.0	Copy from M61PME-S2P 1.0H BOM, only change NB chipset.
2009.10.20	1.0A E_BOM issue	PCB:1.0	change back to W83303+W83320
2010.04.09	2.0A_BOM issue	PCB:2.0	ADD EC FUNCTION / 開機CLSER CMOS PATCH SCHMATIC / EMI PATCH SCHMATIC (DBIOS_RST)
2010.04.28	2.3A_BOM issue	PCB:2.3	DEL IT8590 SCHMATIC , ADD EC FUNCTION(FOR BIOS CONTROL)
2010.06.29	2.3F_BOM issue	PCB:2.3	Change CODEC to ALC888B-VD2-GR

Circuit or PCB layout change for next version

Date	Change Item	Reason
2009.10.??	1.0 Gerber Out	Modify from M68M-S2 1.3 EUP version.
2010.04.08	2.0 Gerber Out	Modify form M68M-S2P 1.01 Add EC, 888VD2 colay.
2010.04.28	2.3 Gerber Out	Modify form M68M-S2P 1.01 Add EC

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Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-M68M-S2P | Rev: 2.3

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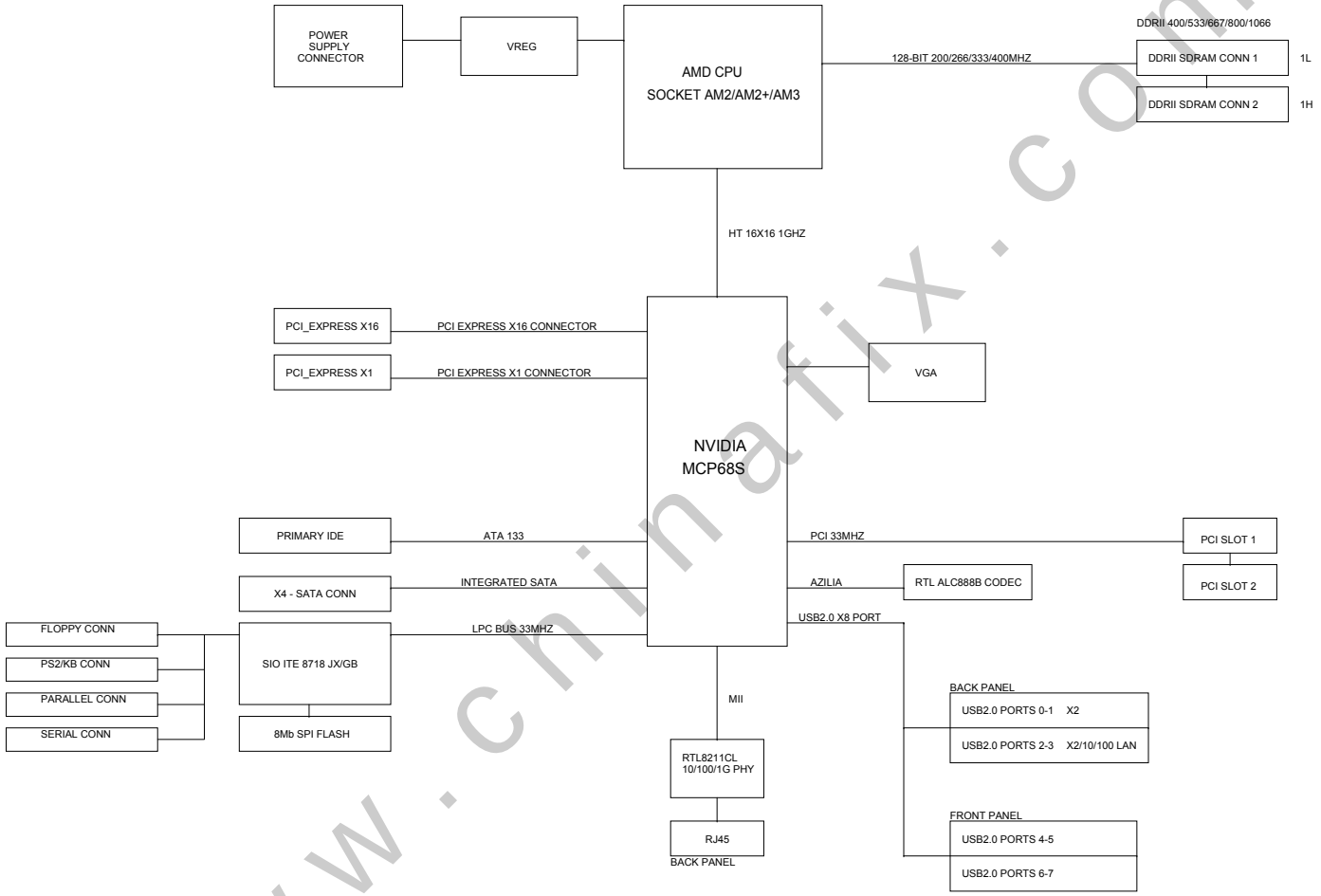
BLOCK DIAGRAM



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<OrgAddr1>	GIGABYTE	
Title	BLOCK DIAGRAM	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 2.3
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] {11}
L0_CADIN_H[0..15] L0_CADIN_H[0..15] {11}
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] {11}
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] {11}
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] {11}
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] {11}
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] {11}
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] {11}

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1
L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1
L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0
L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0
VCC12_HT R3 49.9/4/1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	
GND R4 49.9/4/1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	
{11} L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0
{11} L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0
L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15
L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15
L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14
L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14
L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13
L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13
L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12
L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12
L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11
L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11
L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10
L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10
L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9
L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9
L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8
L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8
L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7
L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7
L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6
L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6
L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5
L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5
L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4
L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4
L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3
L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3
L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AE1	L0_CADOUT_H2
L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AF1	L0_CADOUT_L2
L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1
L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1
L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0
L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0

{11} L0_CTLOUT_H0
{11} L0_CTLOUT_L0

M2CPU

AM2RM/PP/BU/PB/[12KRC-04K812-11R]

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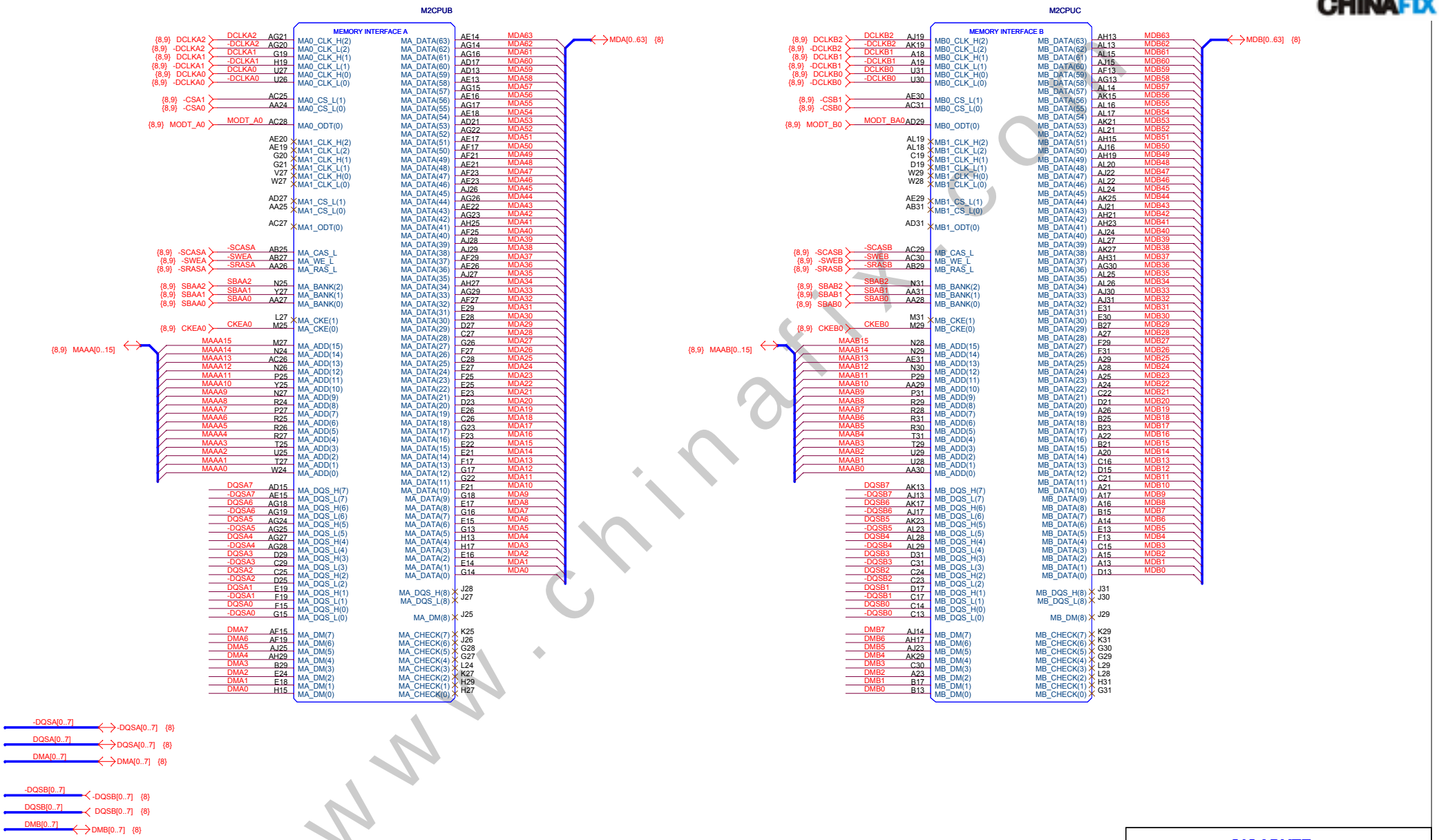
<OrgAddr1>	GIGABYTE	
Title: CPU HYPER TRANSPORT		
Size: Custom	Document Number: GA-M68M-S2P	Rev: 2.3
Date: Tuesday, June 29, 2010	Sheet 4 of 28	



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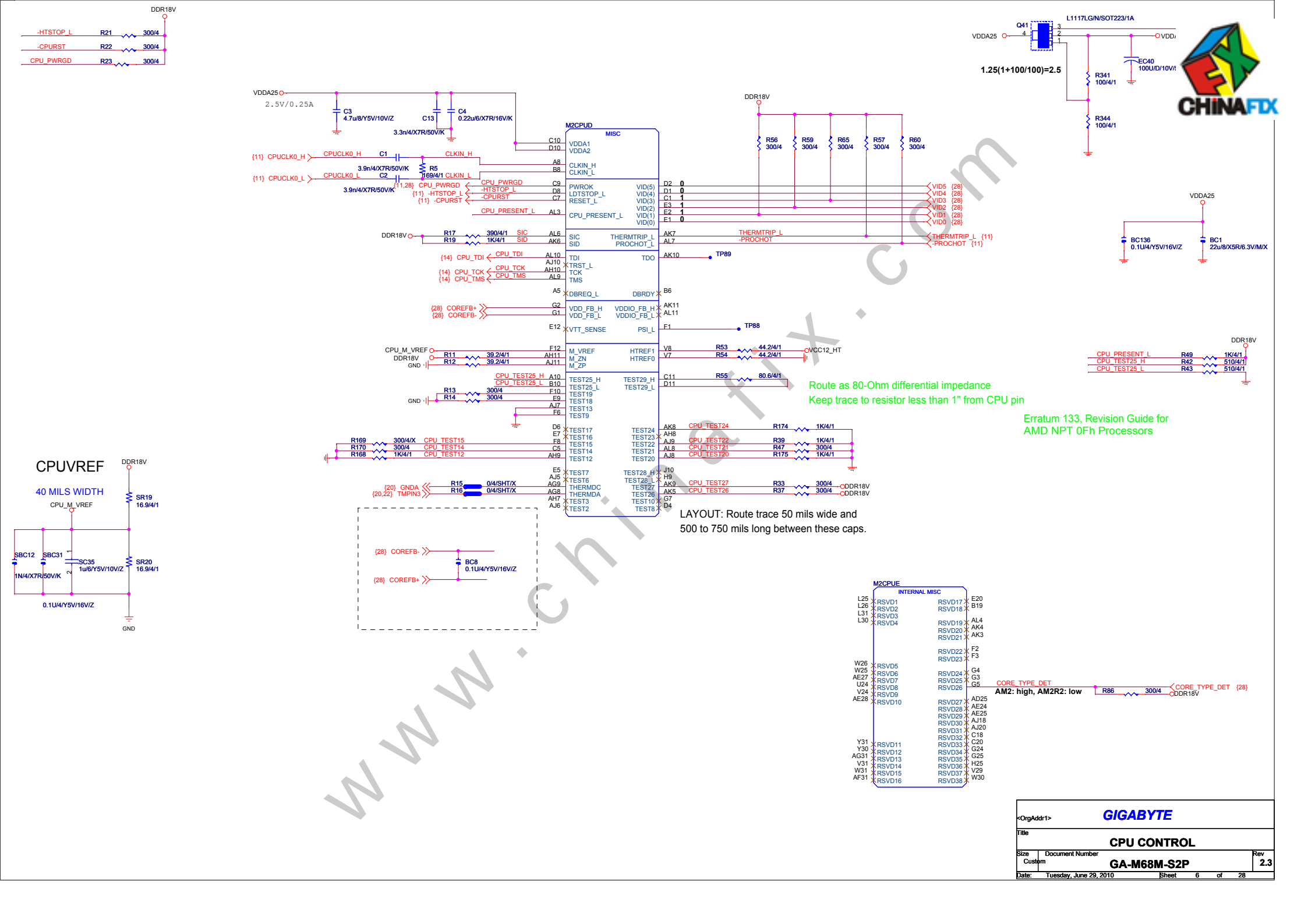
<OrgAddr1>	GIGABYTE		
Title	CPU DDRII MEMORY		
Size: Custom	Document Number: GA-M68M-S2P	Rev: 2.3	
Date: Tuesday, June 29, 2010	Sheet 5 of 28		



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<OrgAddr1>	GIGABYTE	
Title	CPU CONTROL	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 2.3
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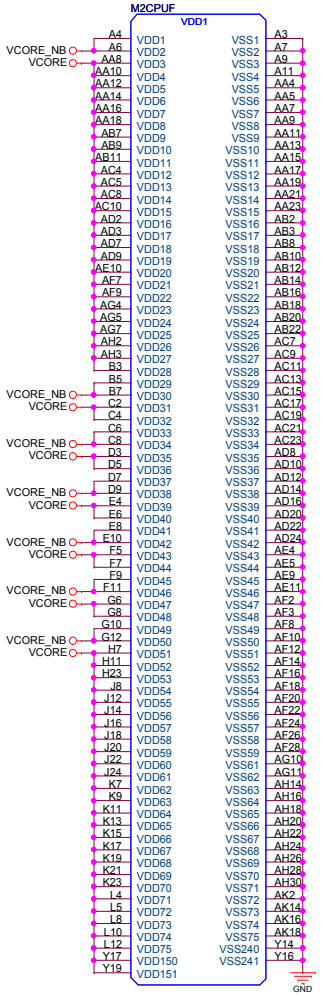
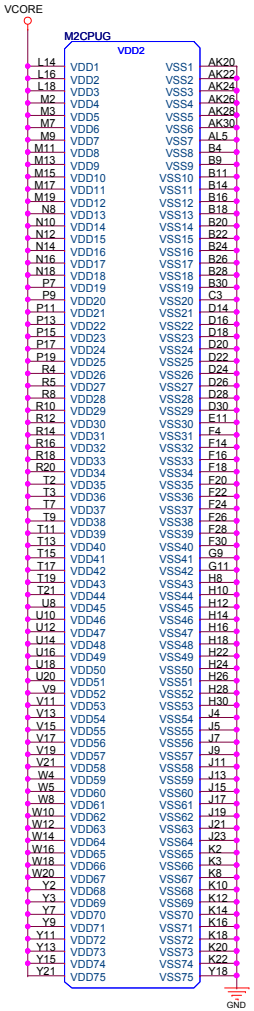
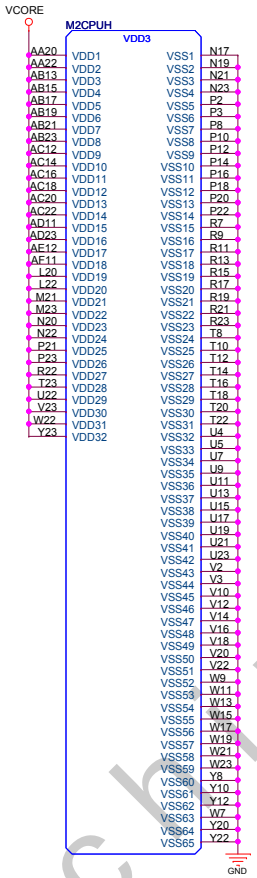
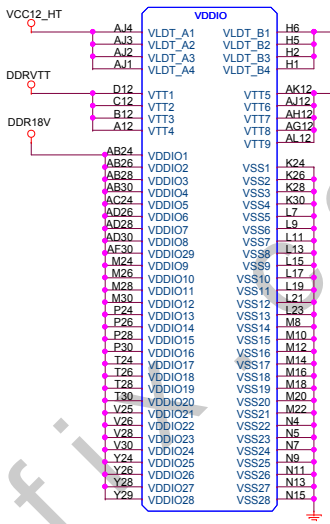
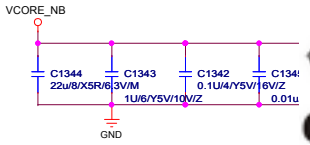
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

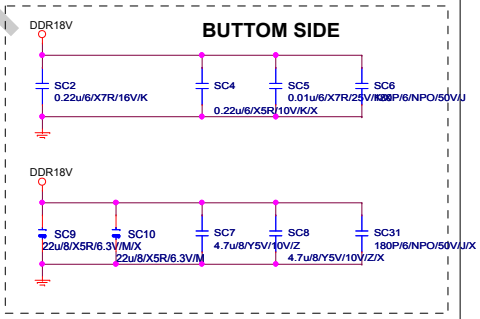


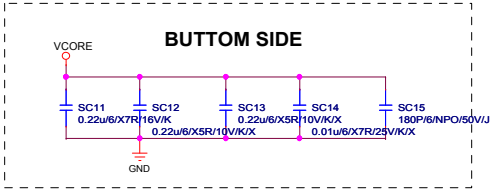


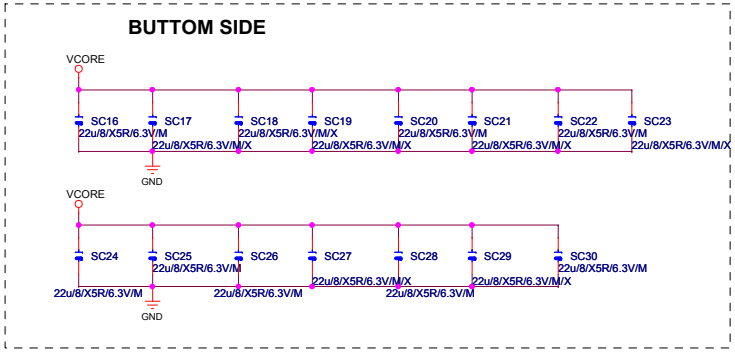


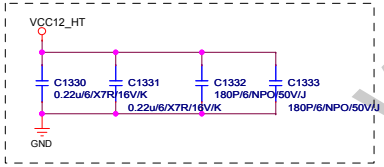


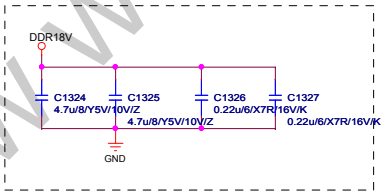


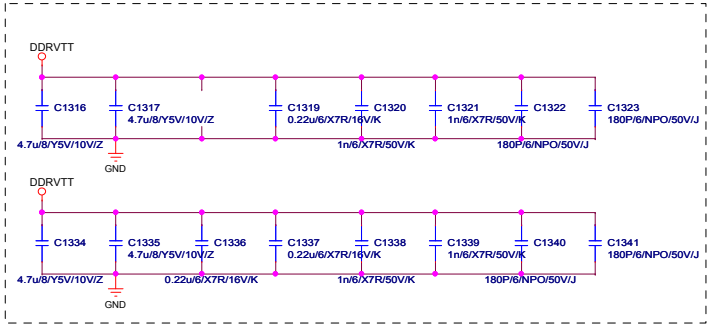












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Title	CPU POWER & GND		
Size: Custom	Document Number: GA-M68M-S2P		Rev: 2.3
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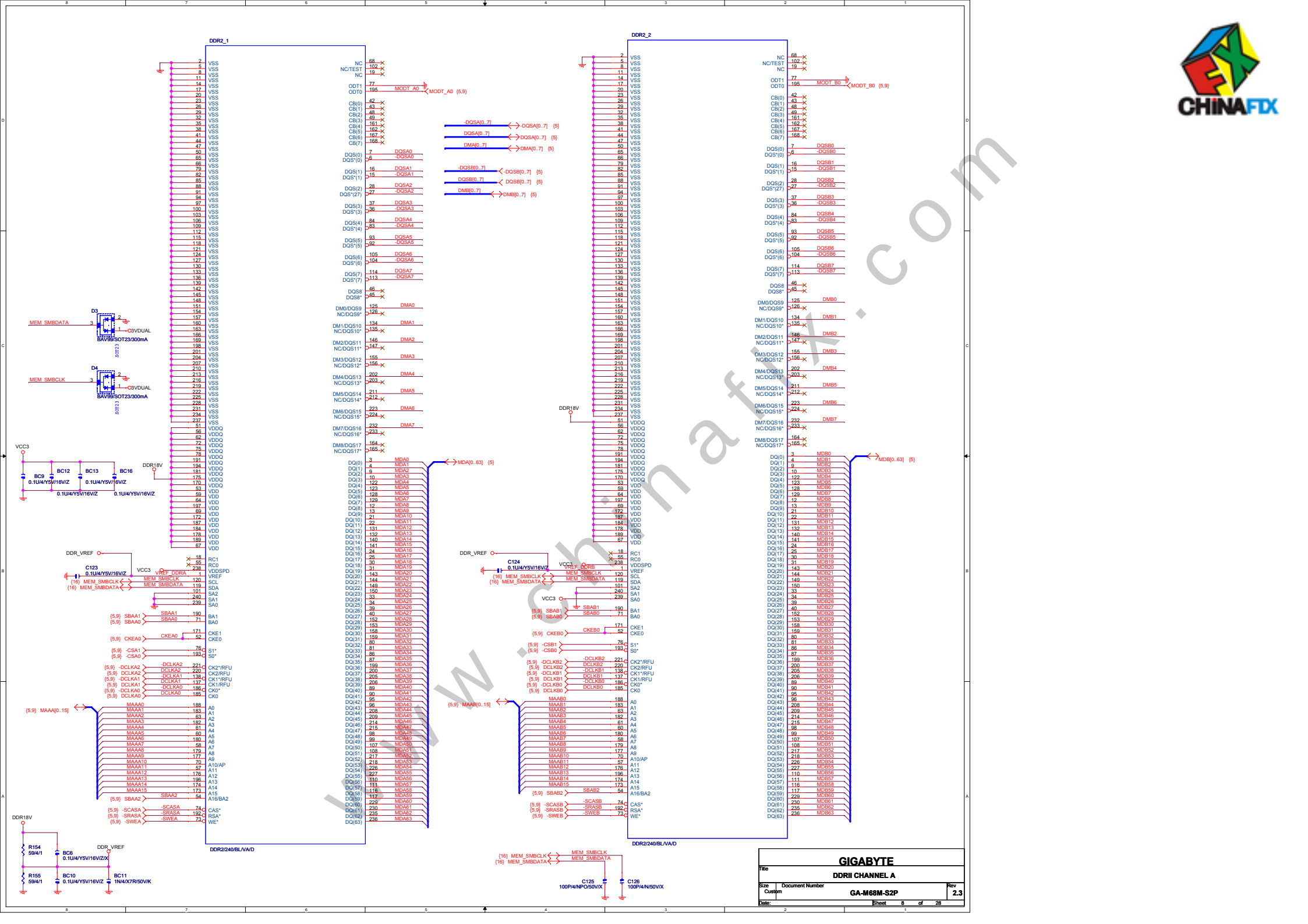

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Title	DDRII CHANNEL A
Size	Custom
Document Number	GA-M68M-S2P
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Date:	Sheet 8 of 28

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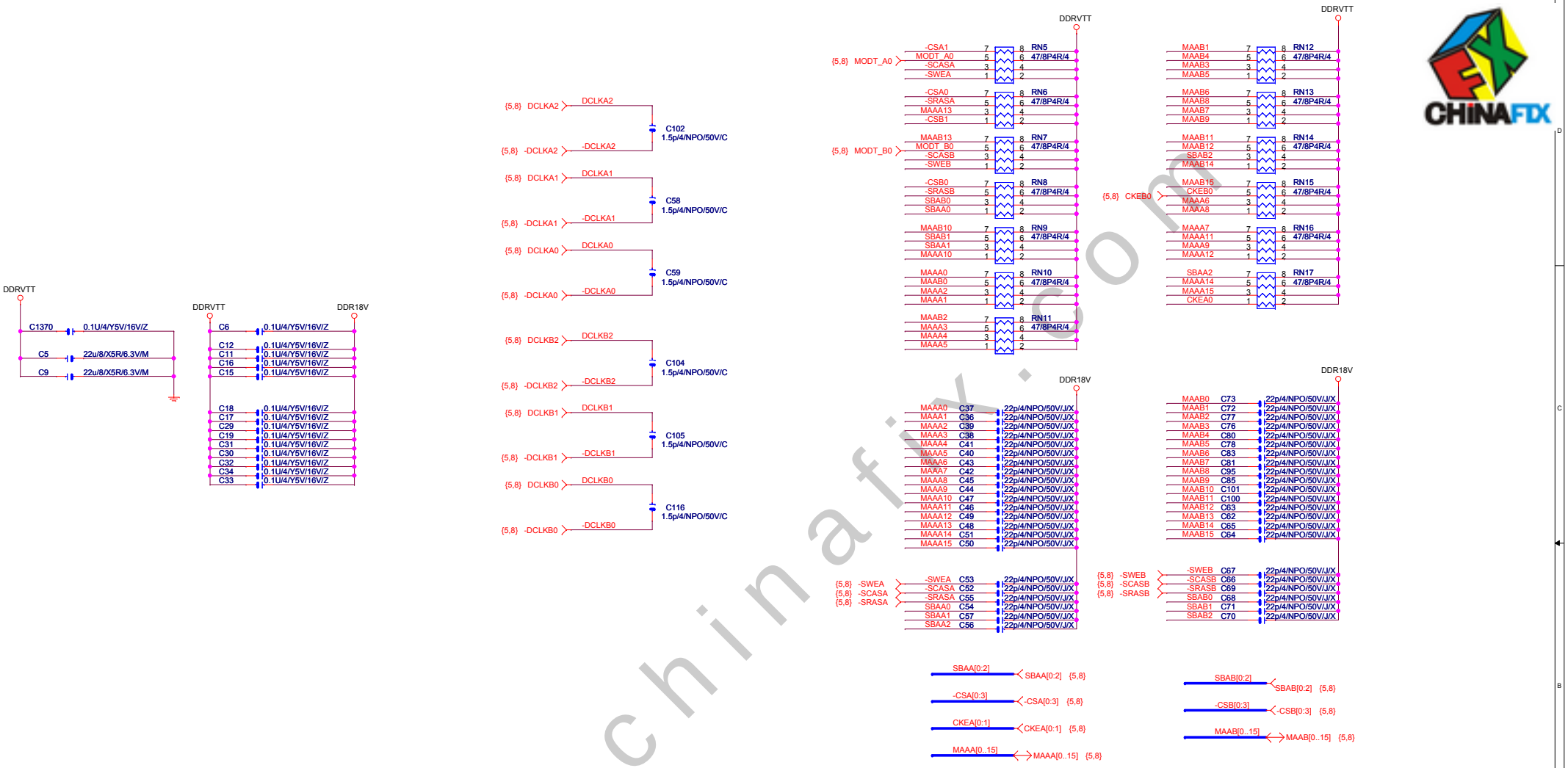

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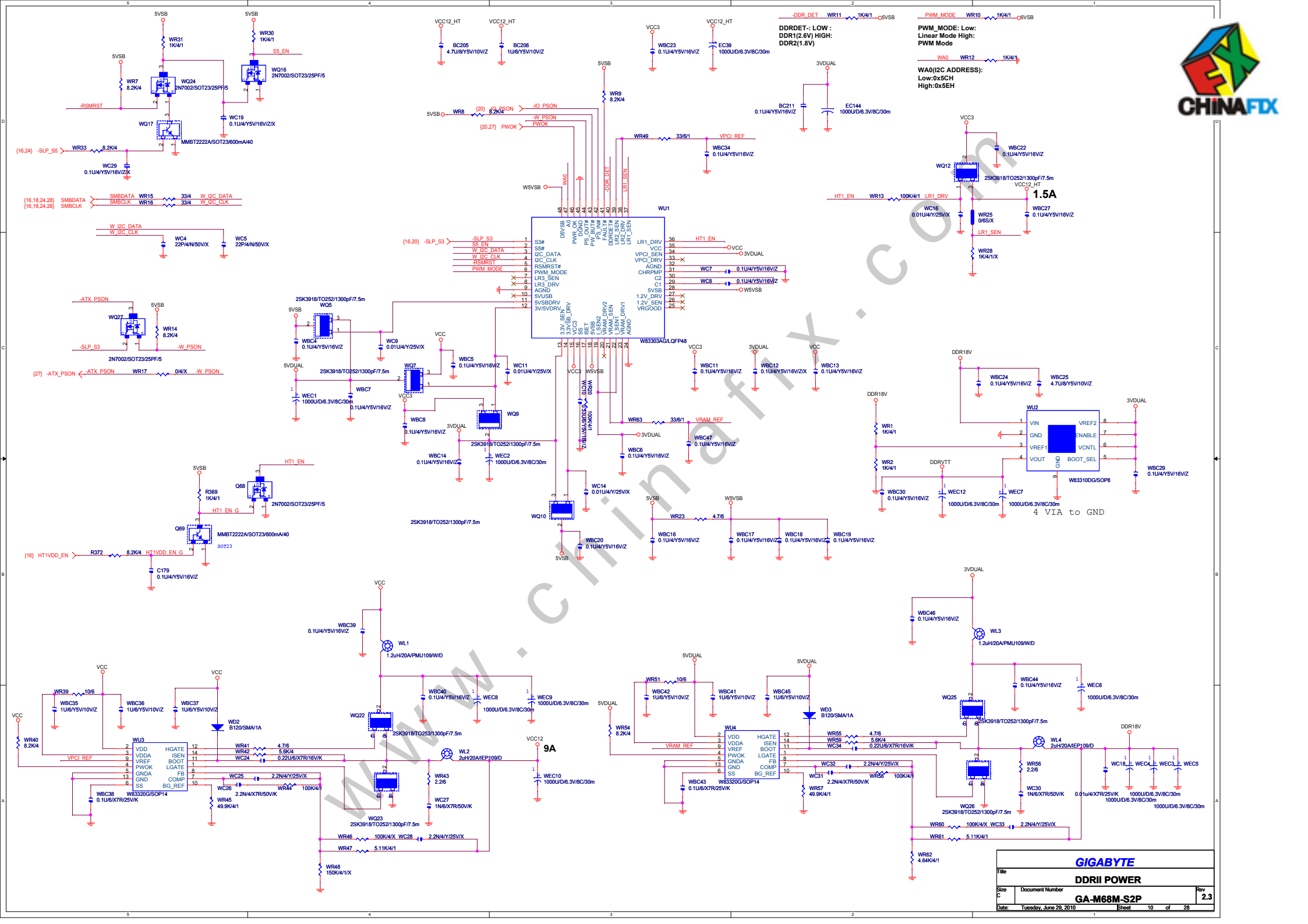
Title	DDRII TERMINATOR	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 2.3
Date: Tuesday, June 29, 2010	Sheet 9 of 28	



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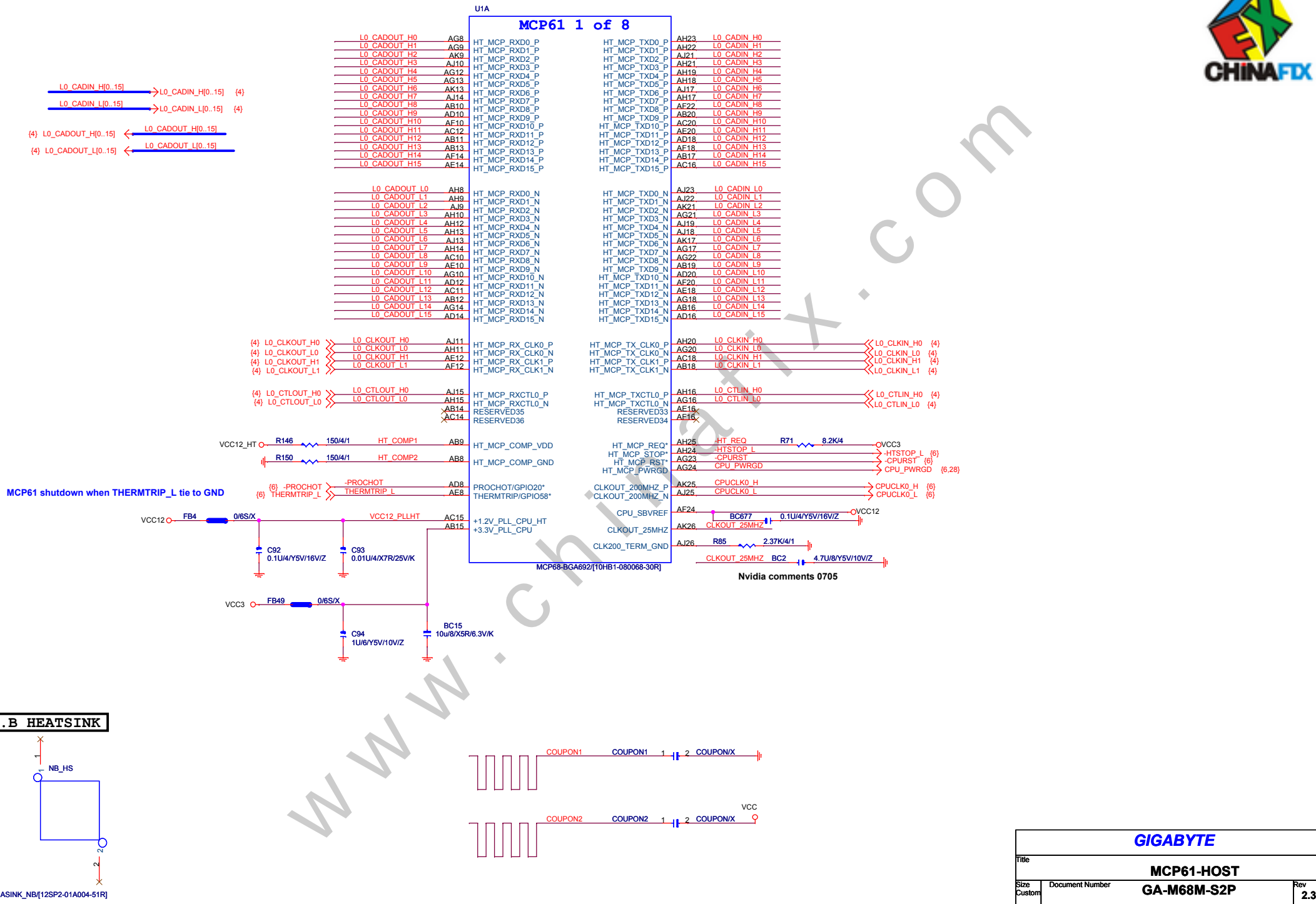

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Title	MCP61-HOST	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 2.3
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Title	MCP61-PCI EXPRESS	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 2.3
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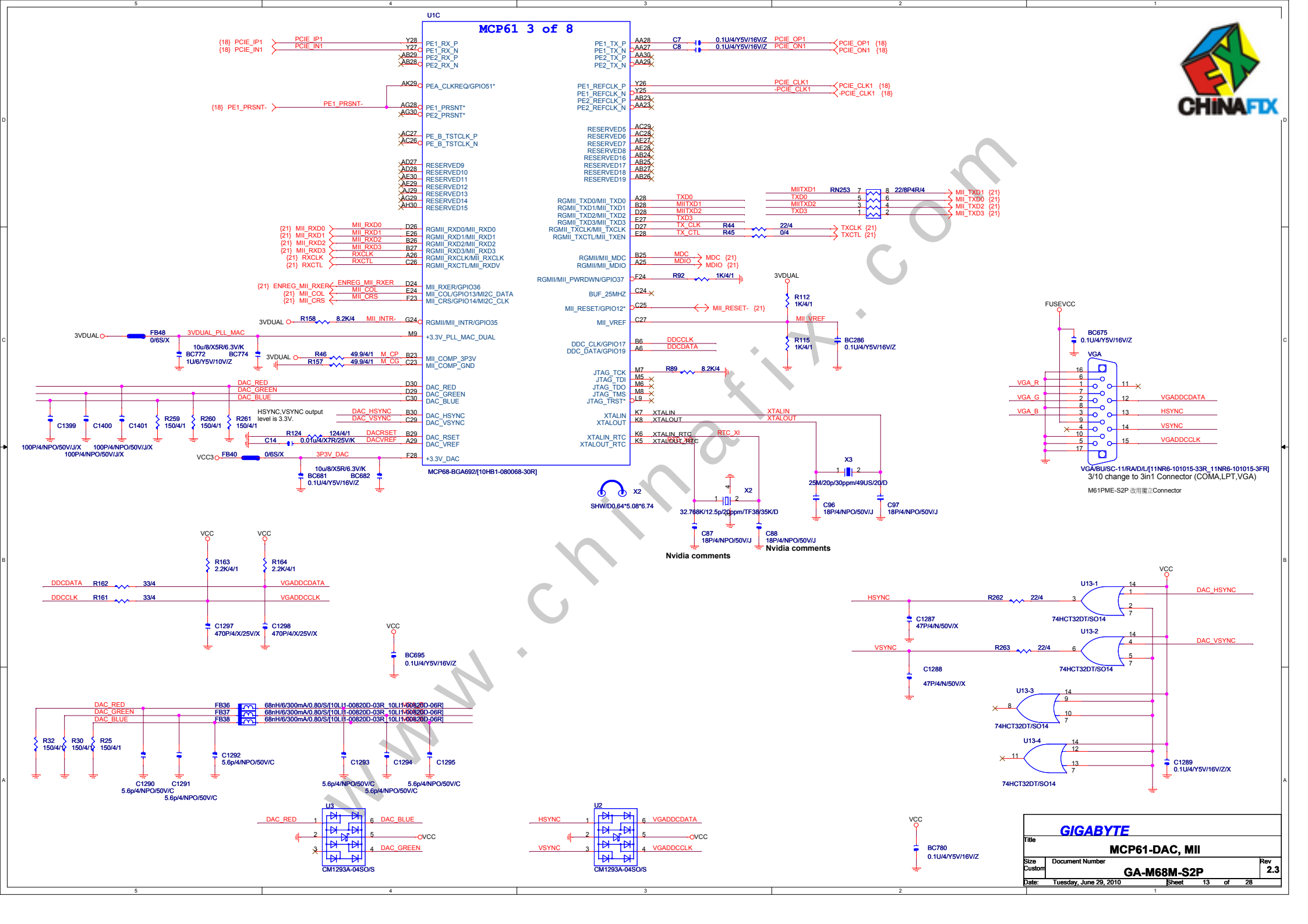

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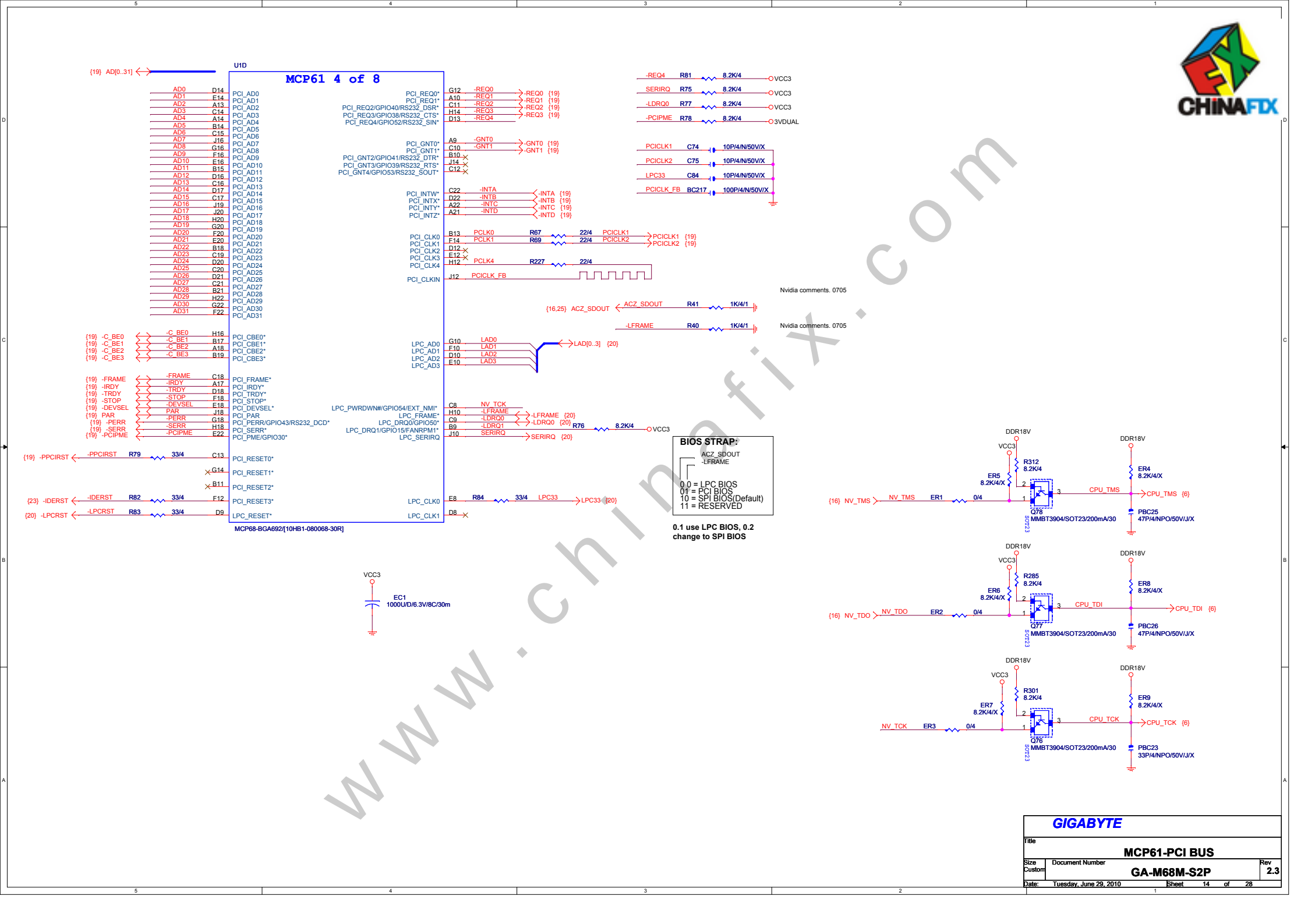

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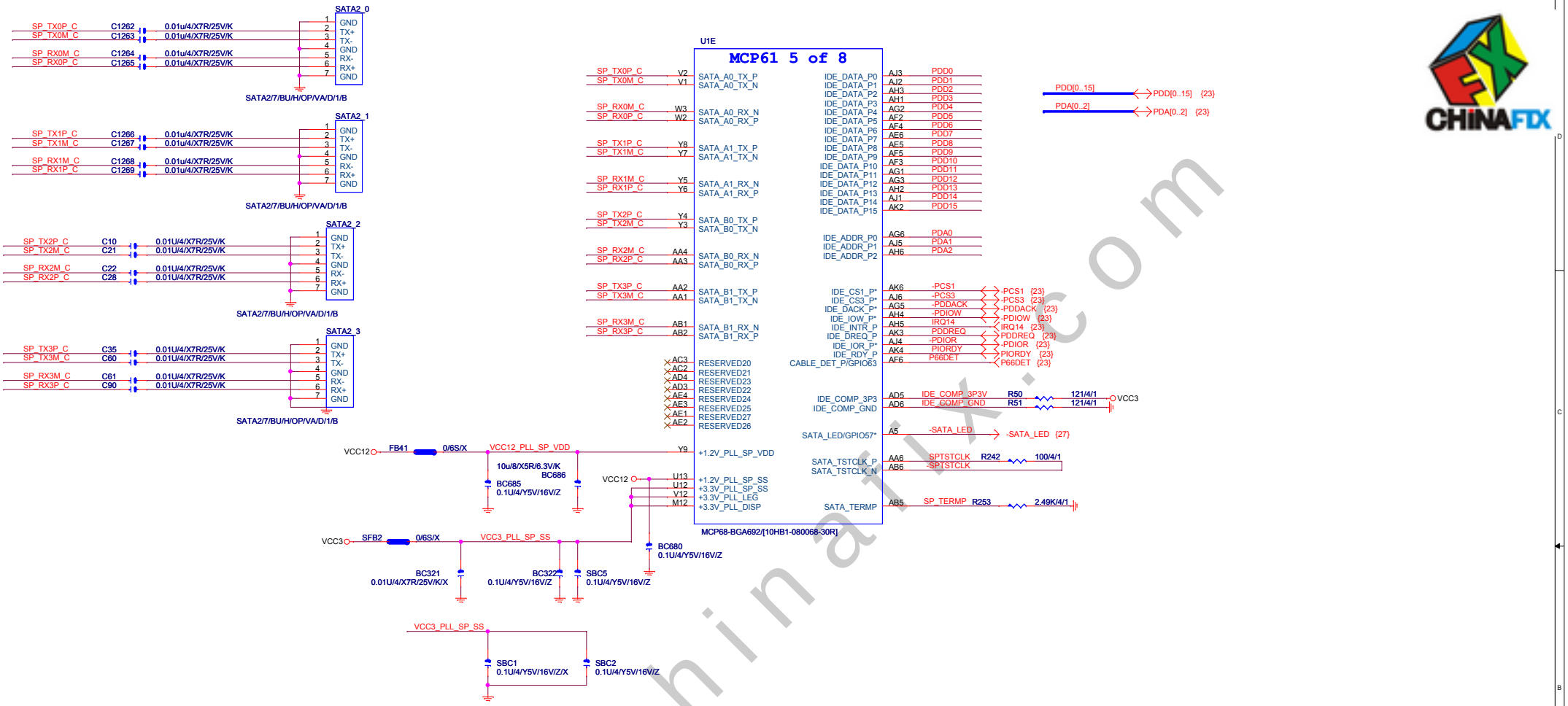
Title	MCP61-PCI BUS	
Size: Custom	Document Number: GA-M68M-S2P	Rev: 2.3
Date: Tuesday, June 29, 2010	Sheet 14 of 28	



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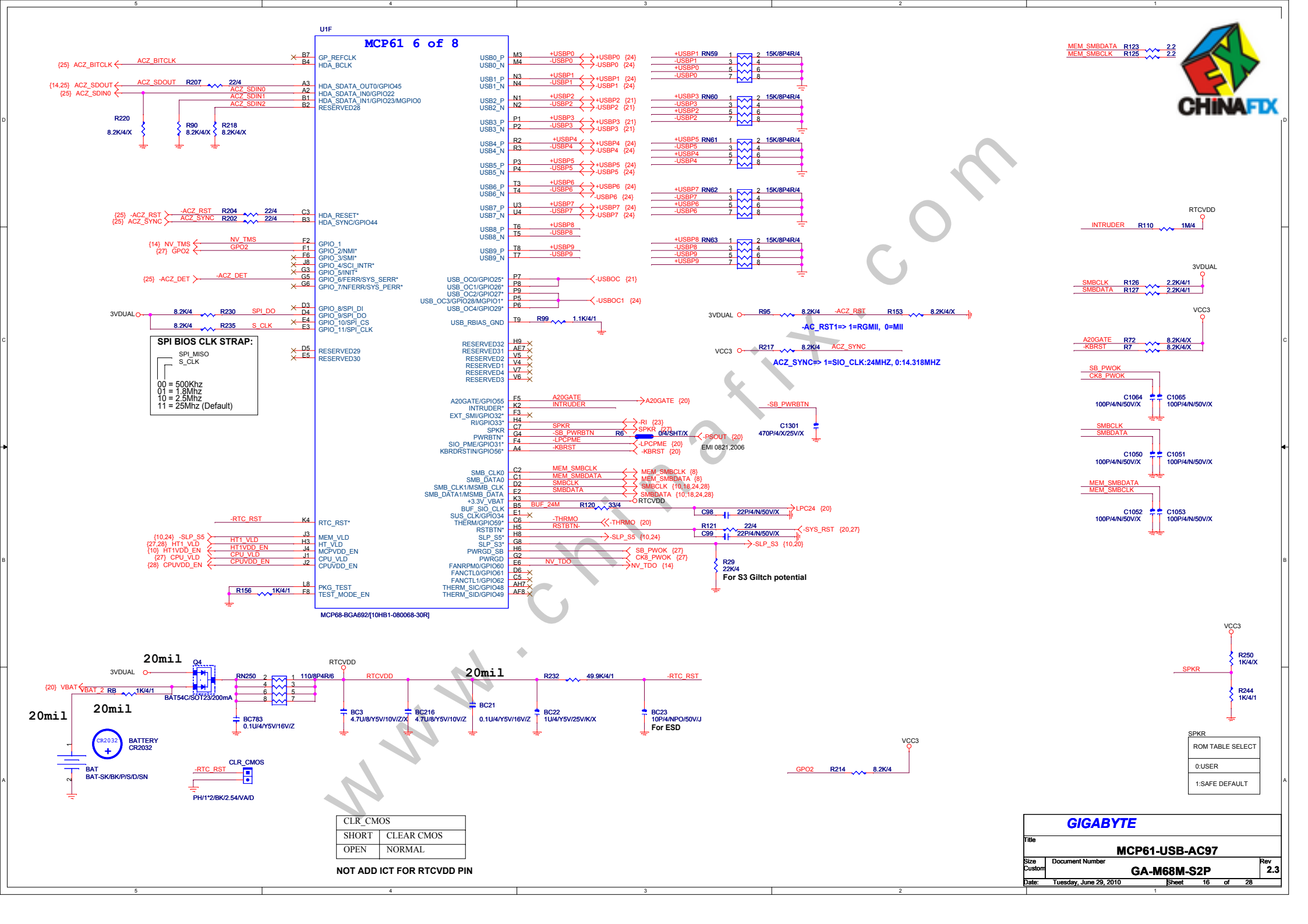
GIGABYTE			
Title: MCP61-SATA/IDE			
Size: Custom	Document Number: GA-M68M-S2P		Rev: 2.3
Date: Tuesday, June 29, 2010	Sheet 15 of 28		



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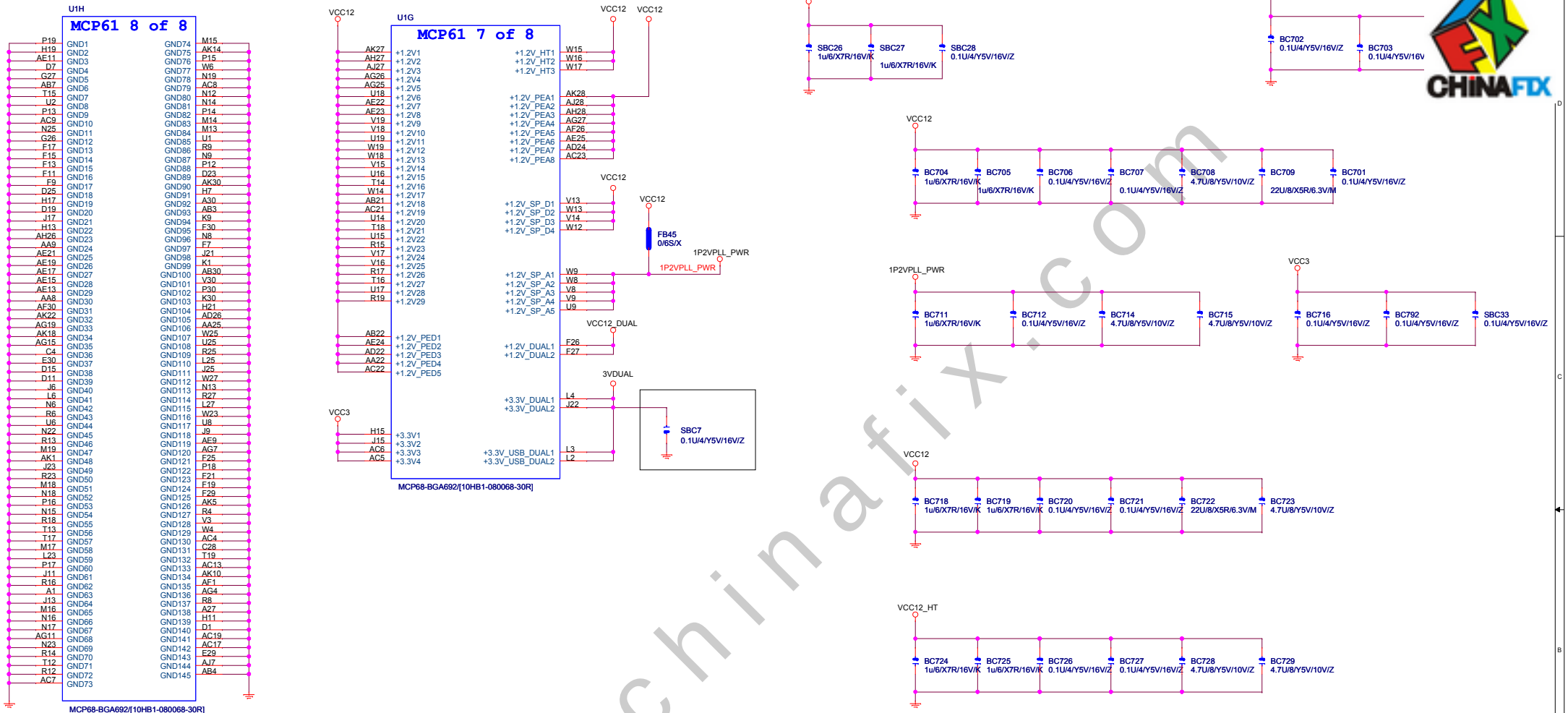

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GIGABYTE			
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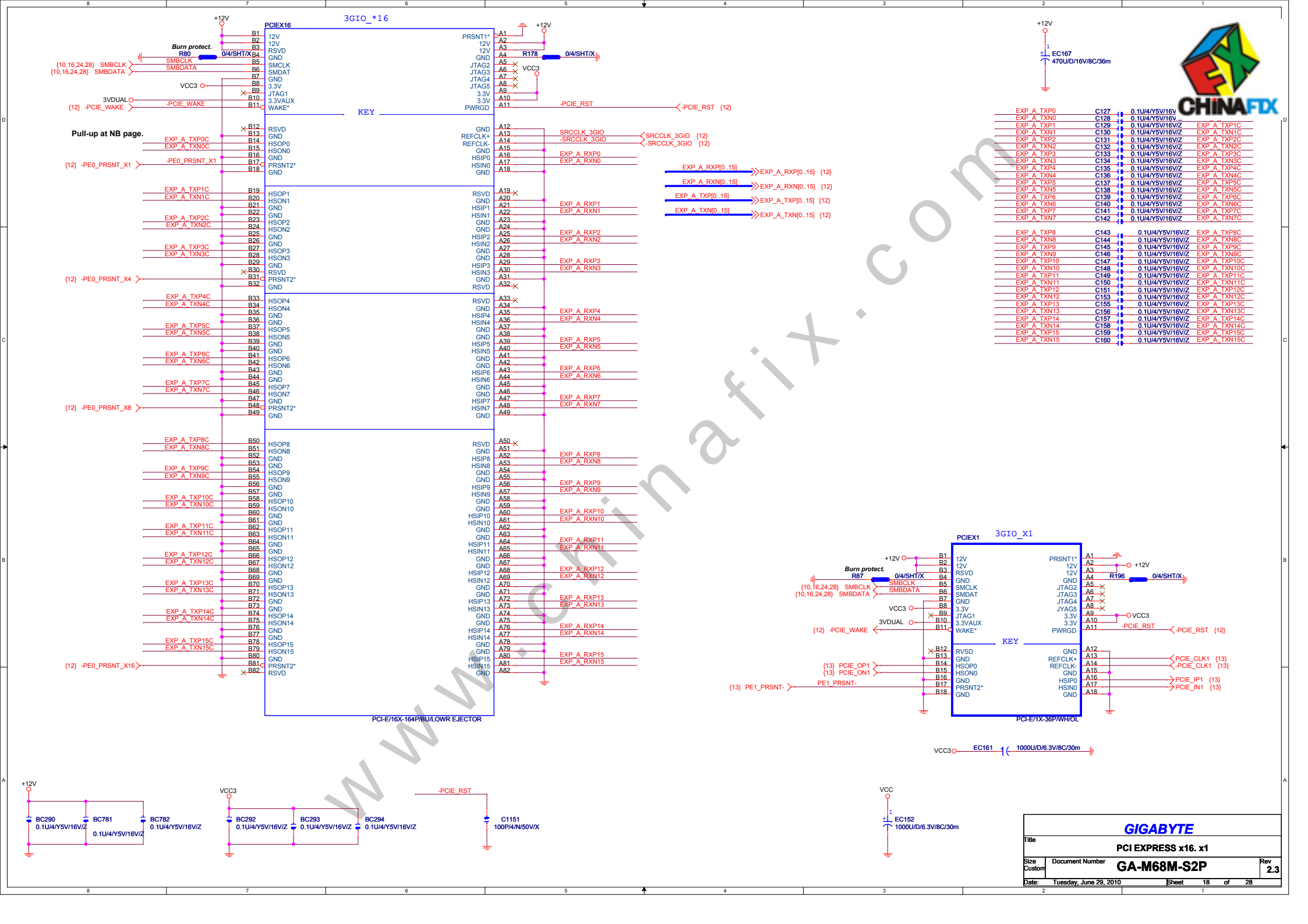
Size: Custom	Document Number: GA-M68M-S2P		Rev: 2.3
Date: Tuesday, June 29, 2010	Sheet 17 of 28		



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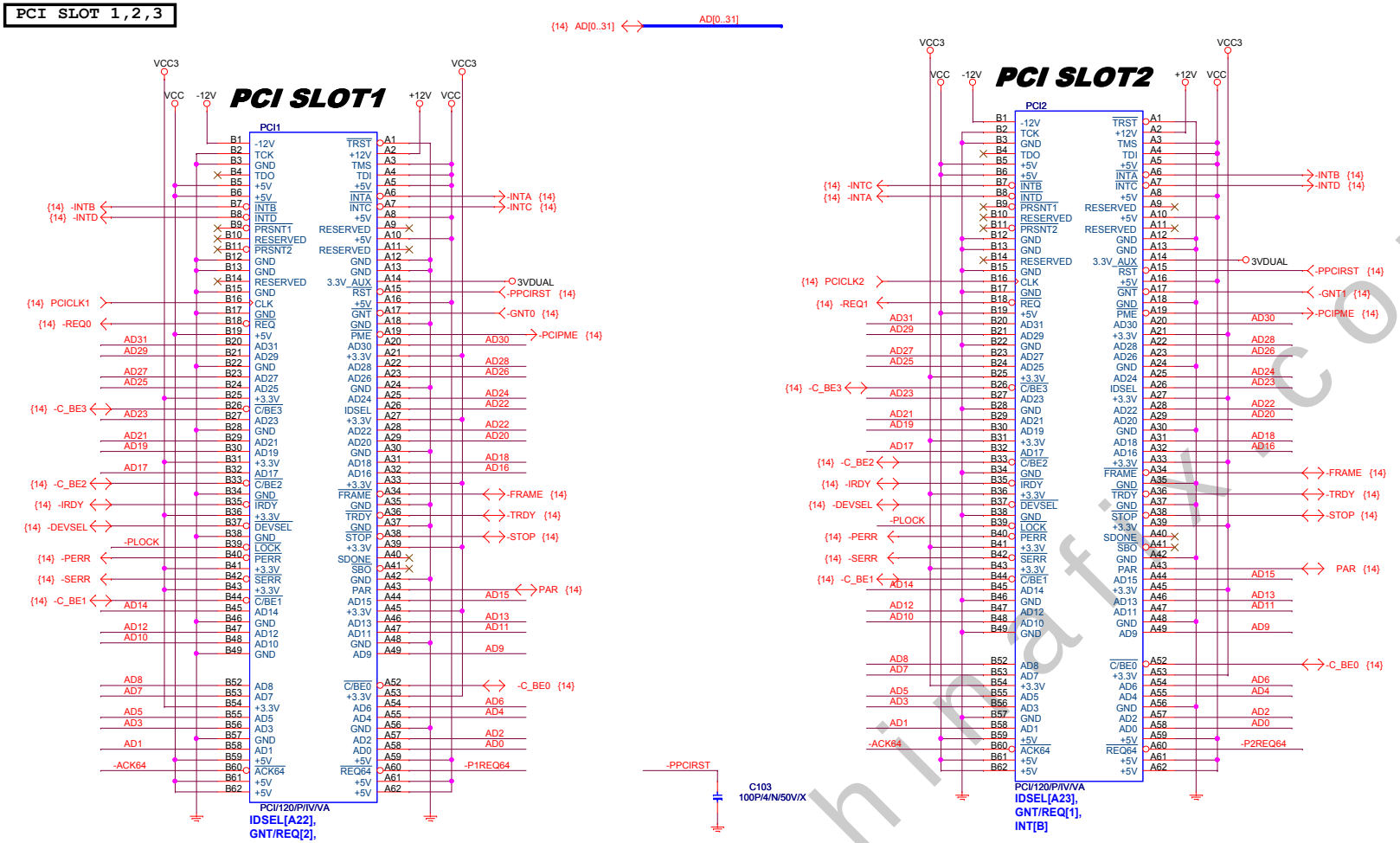
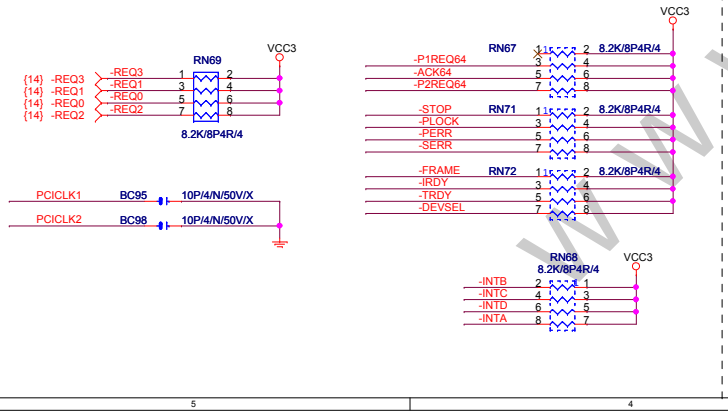
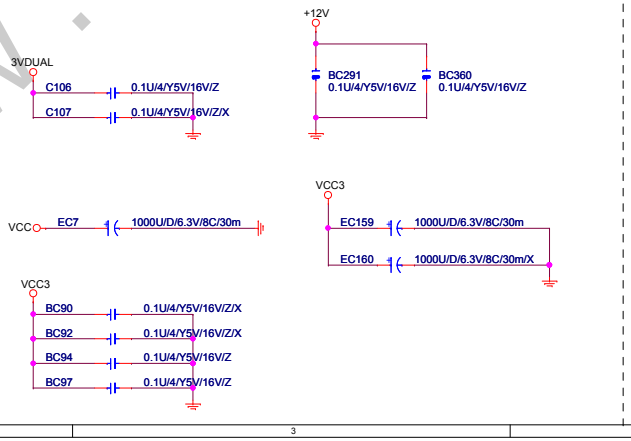
PCI SLOT 1,2,3







Title	GIGABYTE		
	PCI SLOT 1,2		
Size: Custom	Document Number: GA-M68M-S2P		Rev: 2.3
Date: Tuesday, June 29, 2010	Sheet 19 of 28		

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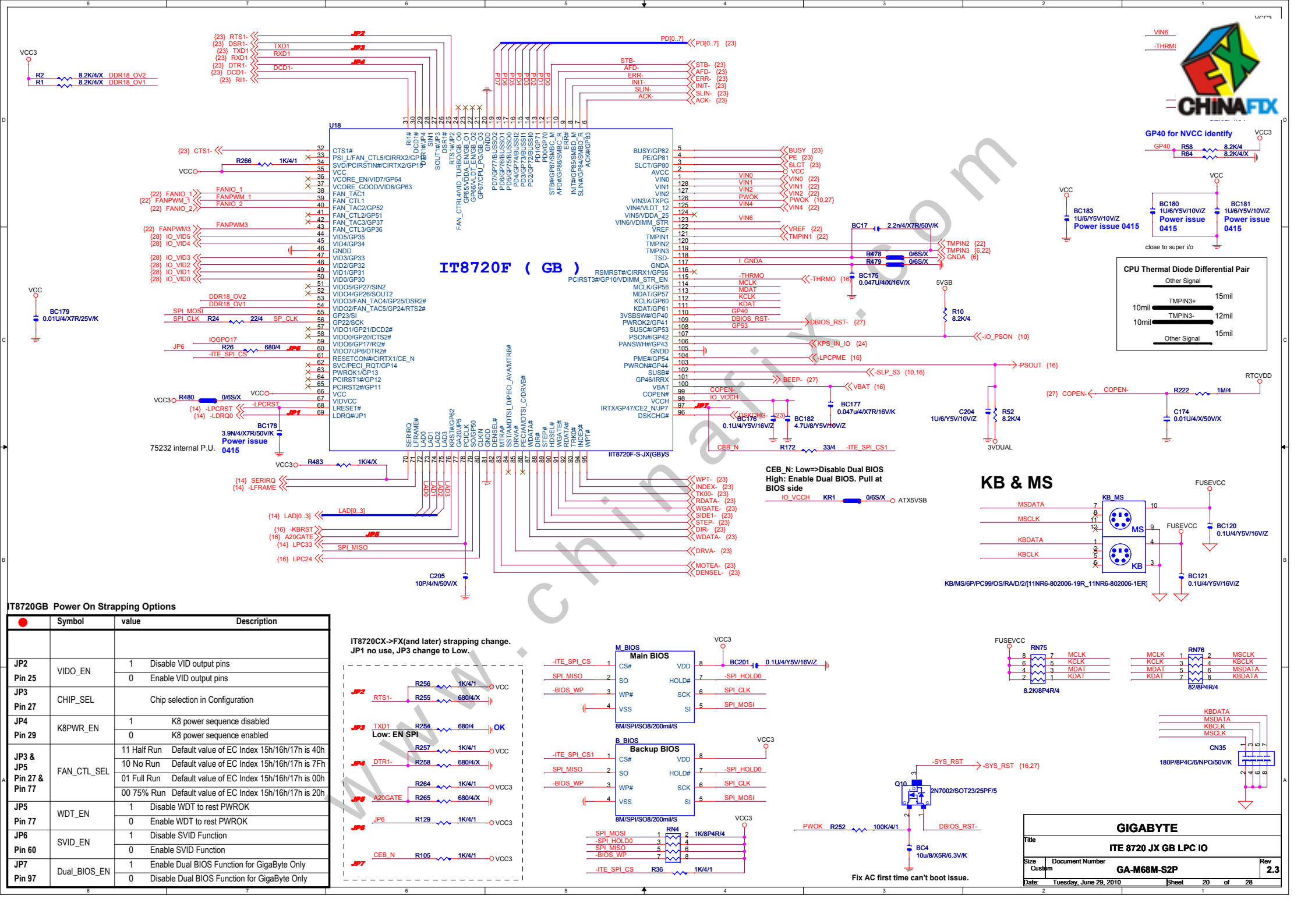

	Symbol	value	Description
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	CHIP_SEL		Chip selection in Configuration
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

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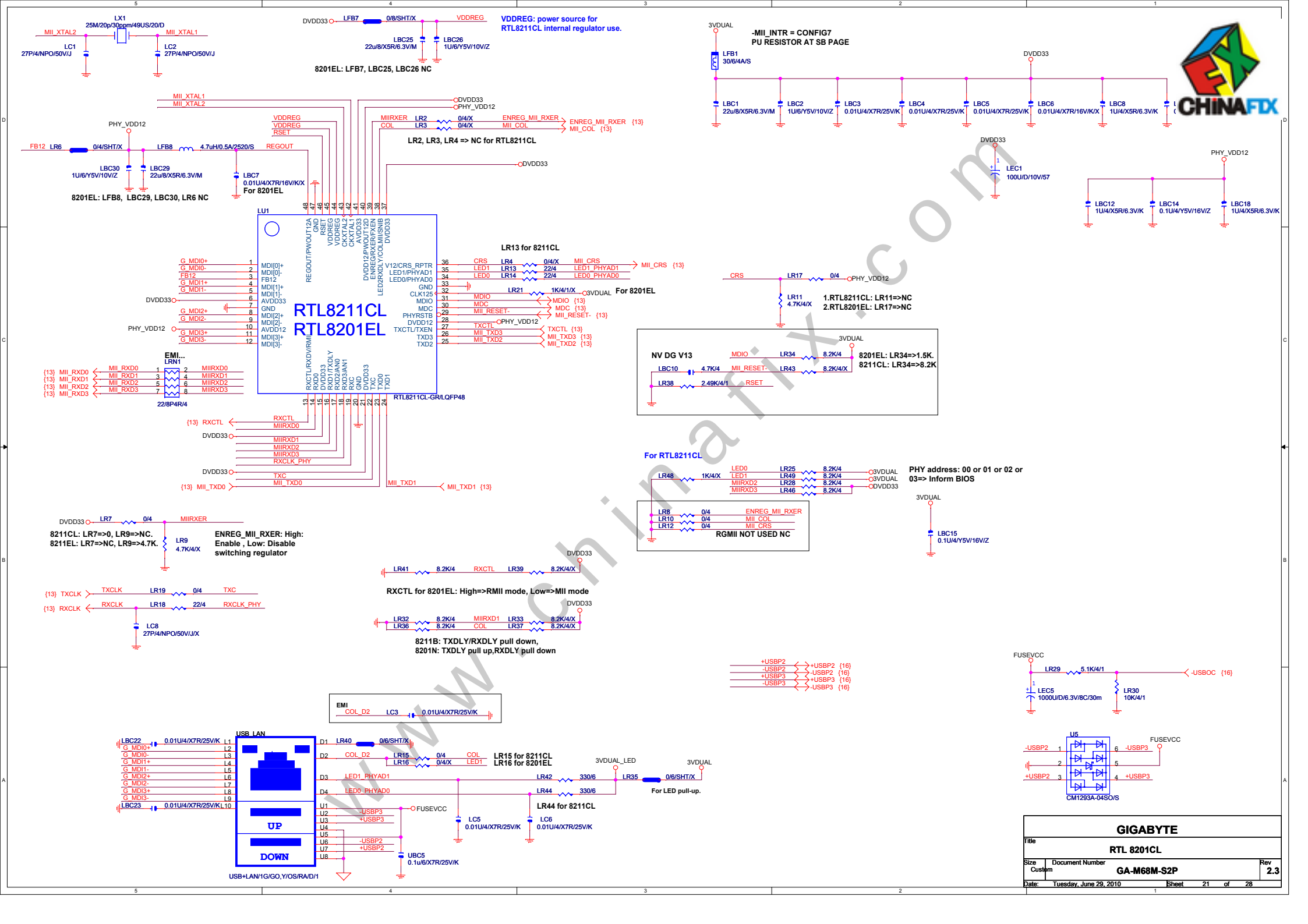

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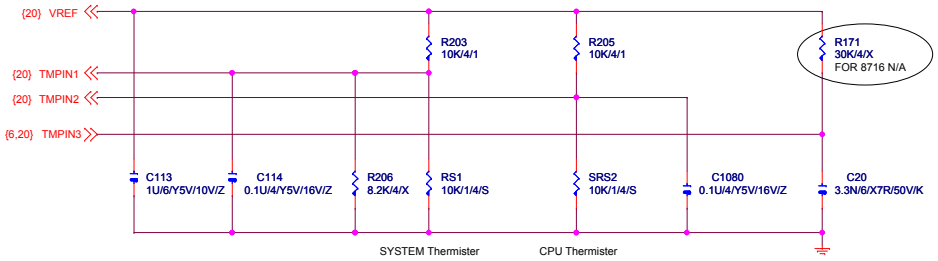
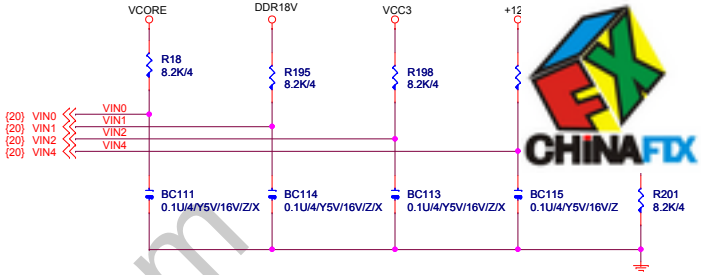
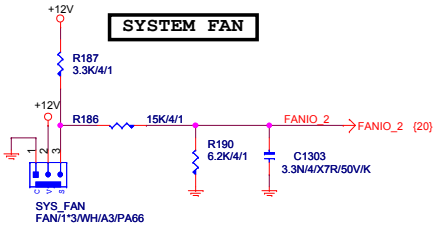
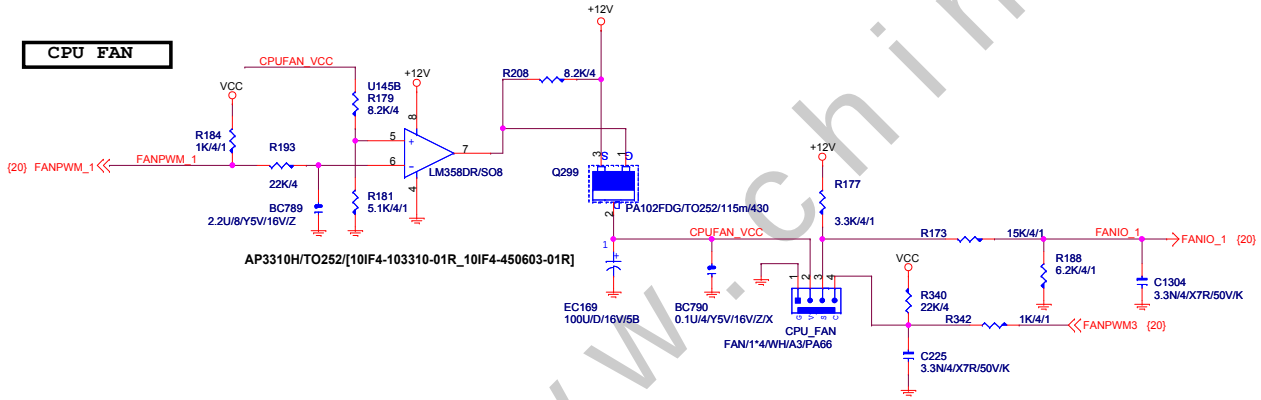
Hardware Monitor circuits









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Title	FAN/HWMO KB/MS	
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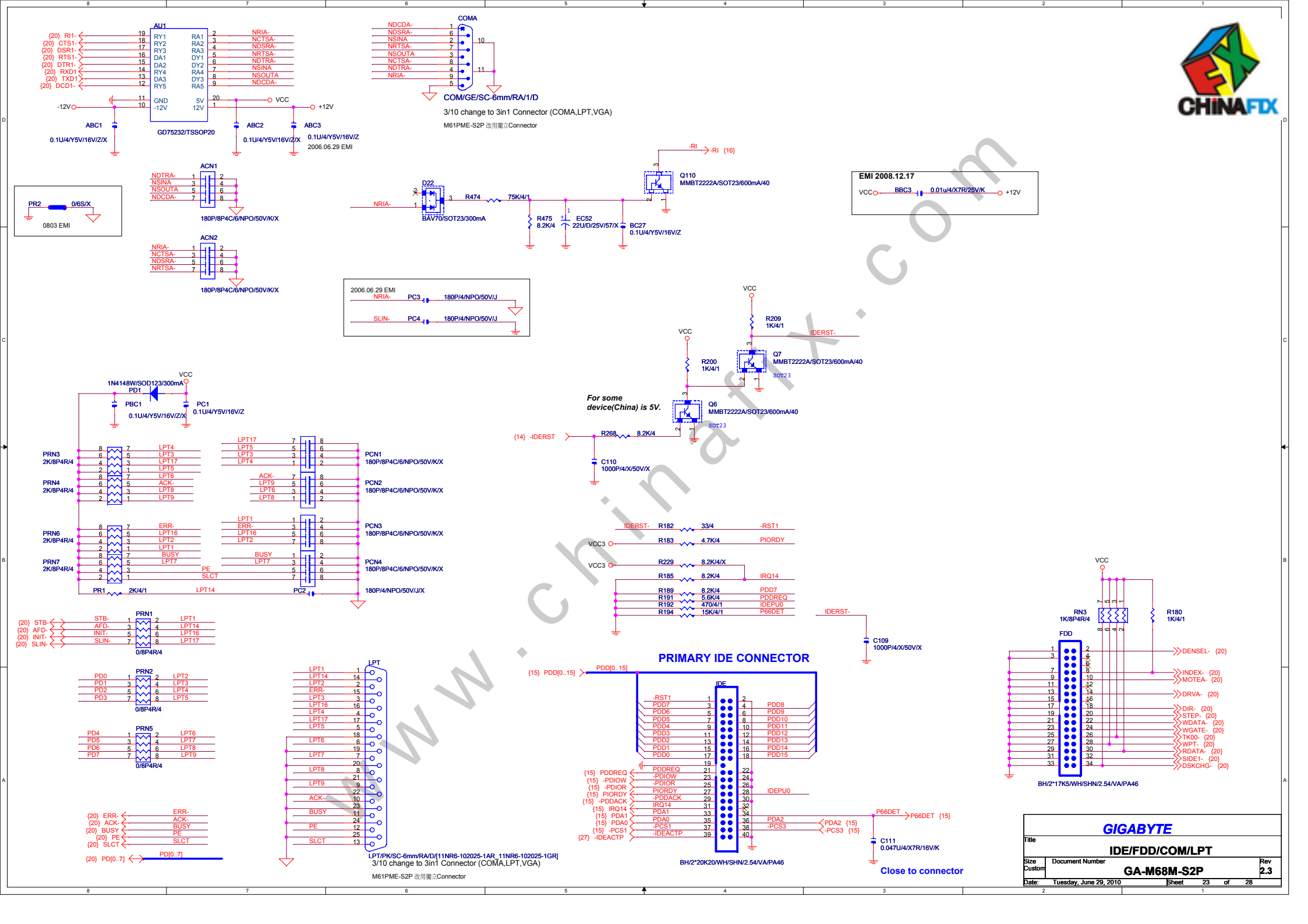

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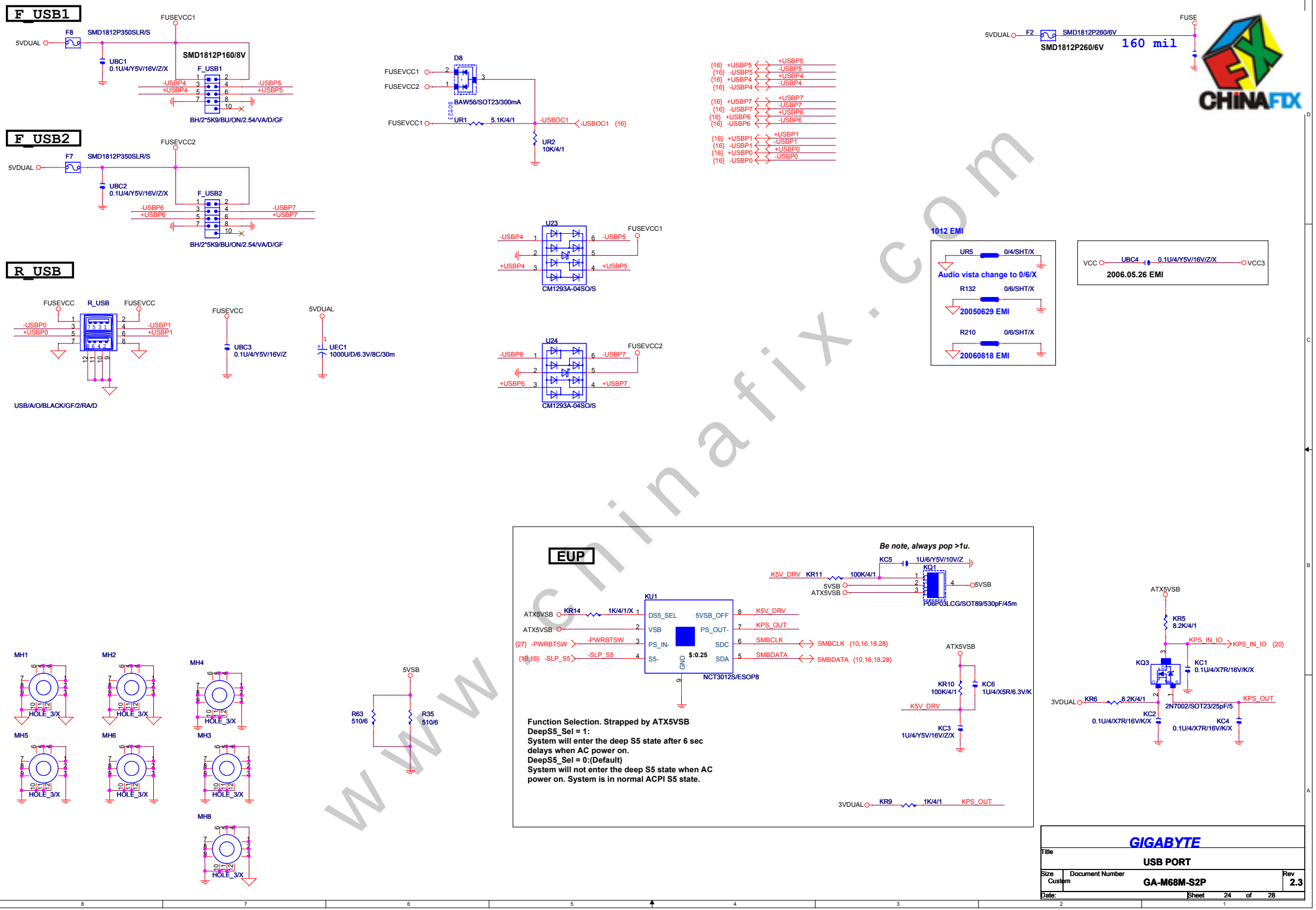

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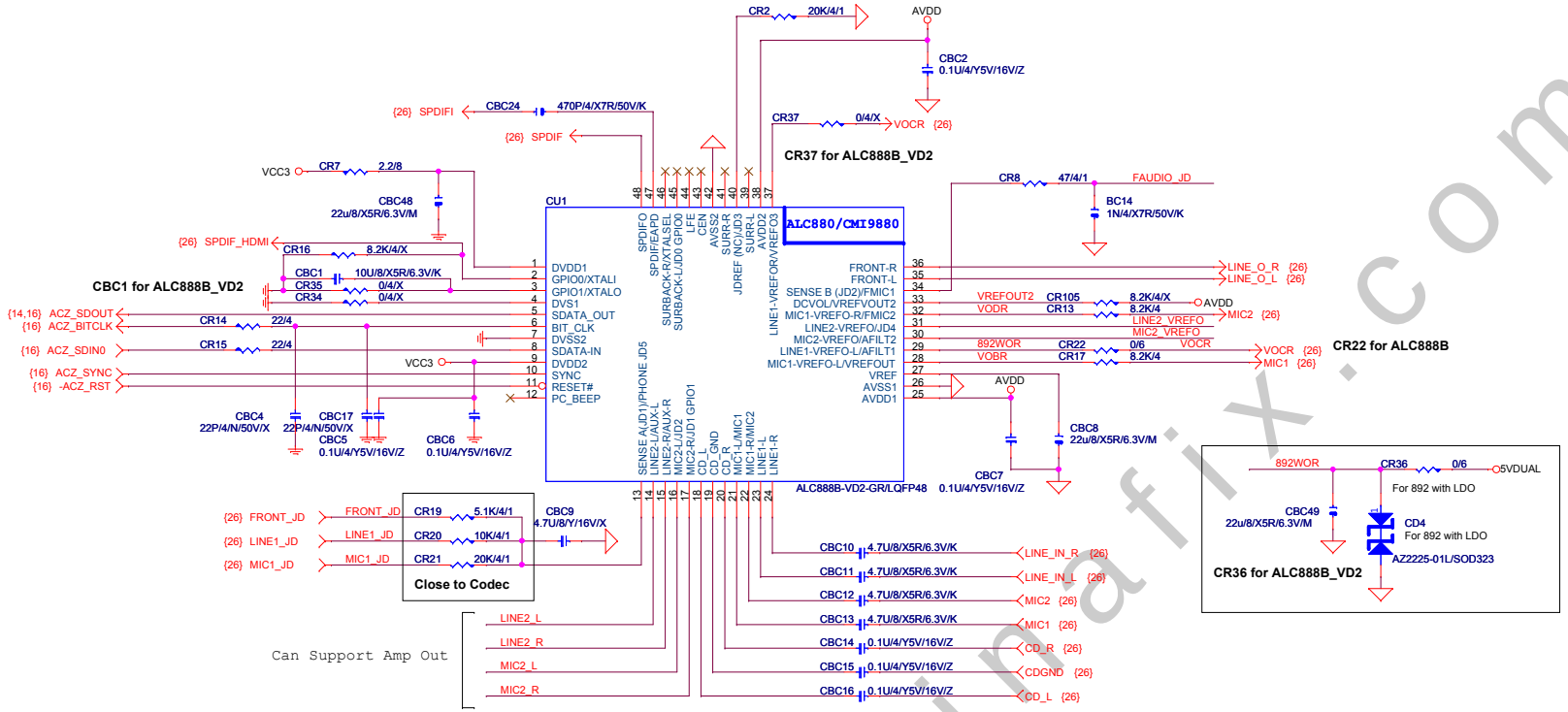

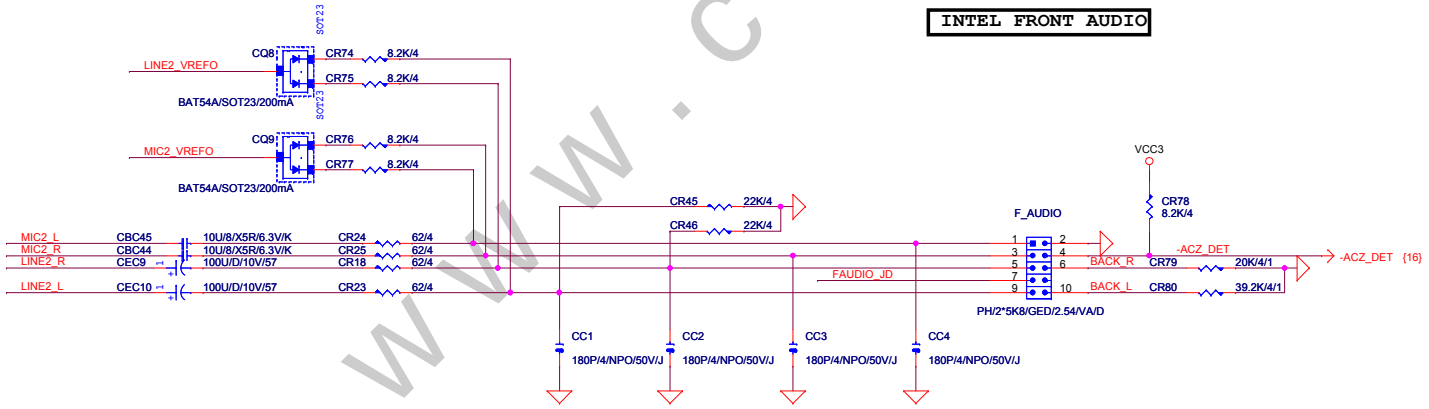

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GIGABYTE		
Title: ALC888		
Size: Custom	Document Number: GA-M68M-S2P	Rev: 2.3
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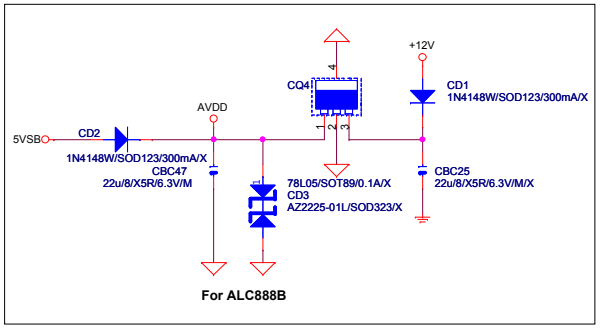
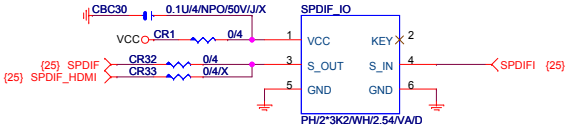
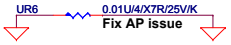
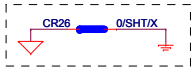
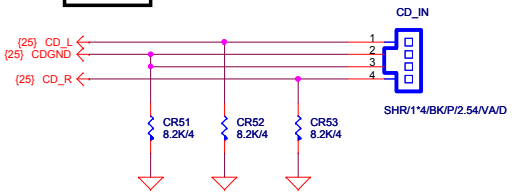


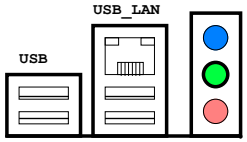


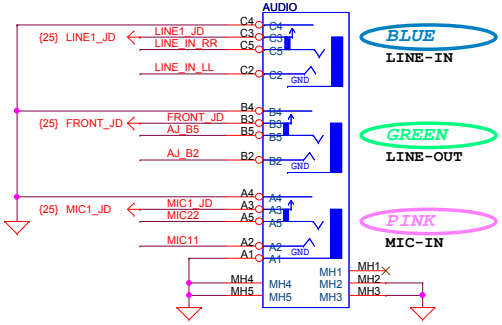




CD IN



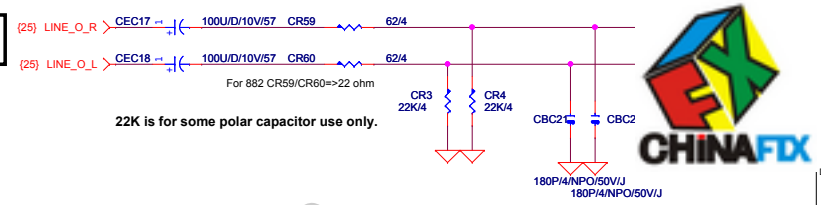




A3RP/13P/BL,LI,PK/RA/D/1/B

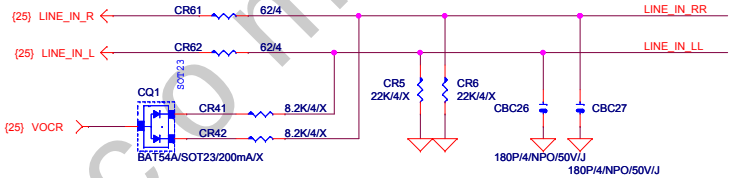
A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15F/[11NR6-403004-11]

LINE OUT
FRONT OUT

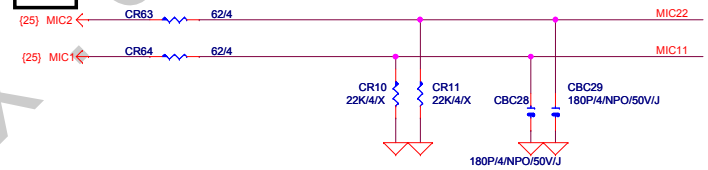


22K is for some polar capacitor use only.

LINE-IN



MIC



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Title	AUDIO JACK		
Size: Custom	Document Number: GA-M68M-S2P		Rev: 2.3
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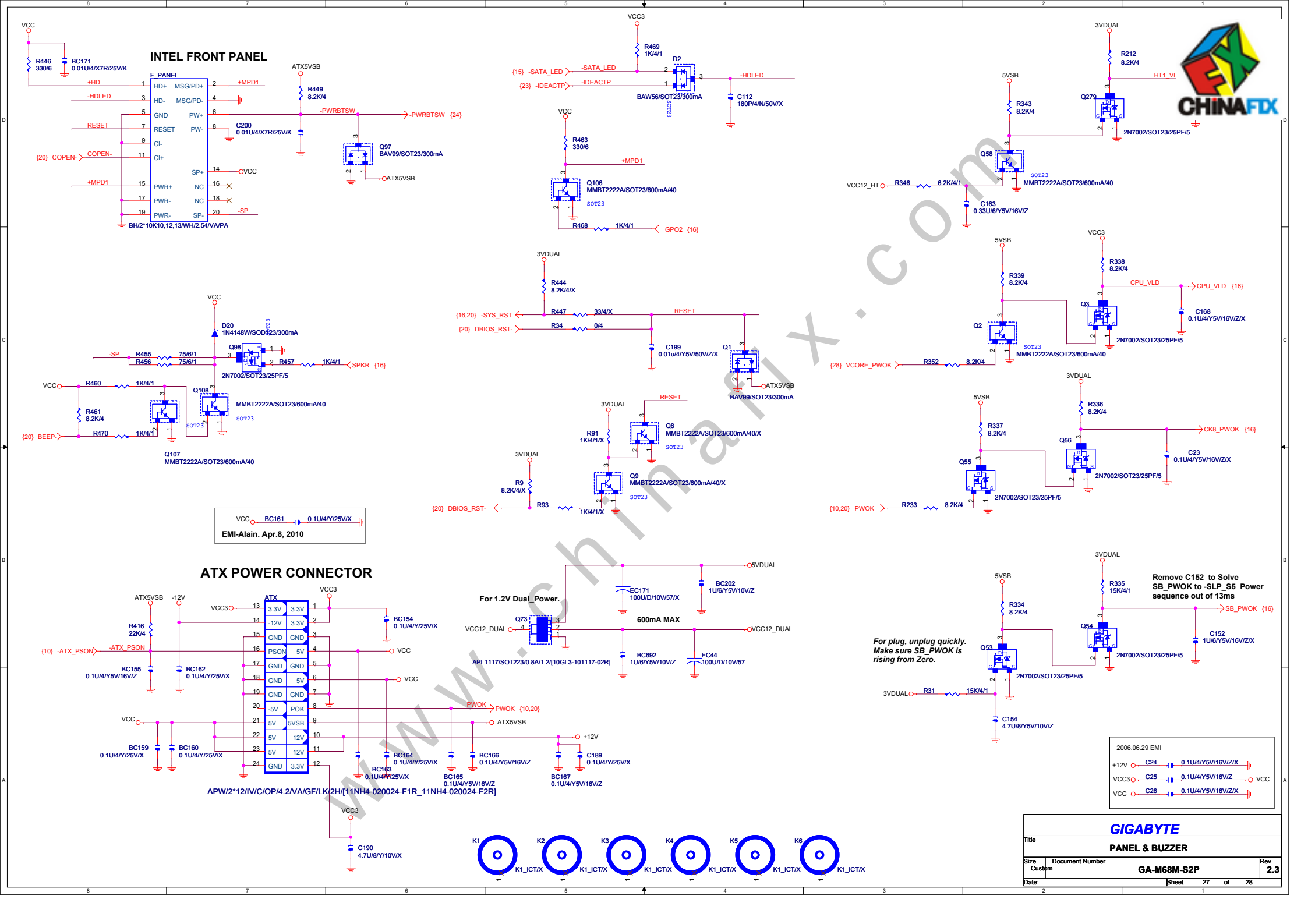
INTEL FRONT PANEL
F_PANEL
BH/2*10K10,12,13/WH/2.54/VA/PA
ATX POWER CONNECTOR
APW/2*12/IV/C/OP/4.2/VA/GF/LK/2H/[11NH4-020024-F1R_11NH4-020024-F2R]
EMI-Alain. Apr.8, 2010
For 1.2V Dual_Power.
600mA MAX
APL1117/SOT223/0.8A/1.2/[10GL3-101117-02R]
Remove C152 to Solve SB_PWOK to -SLP_S5 Power sequence out of 13ms
For plug, unplug quickly. Make sure SB_PWOK is rising from Zero.
2006.06.29 EMI
GIGABYTE
PANEL & BUZZER
GA-M68M-S2P
2.3
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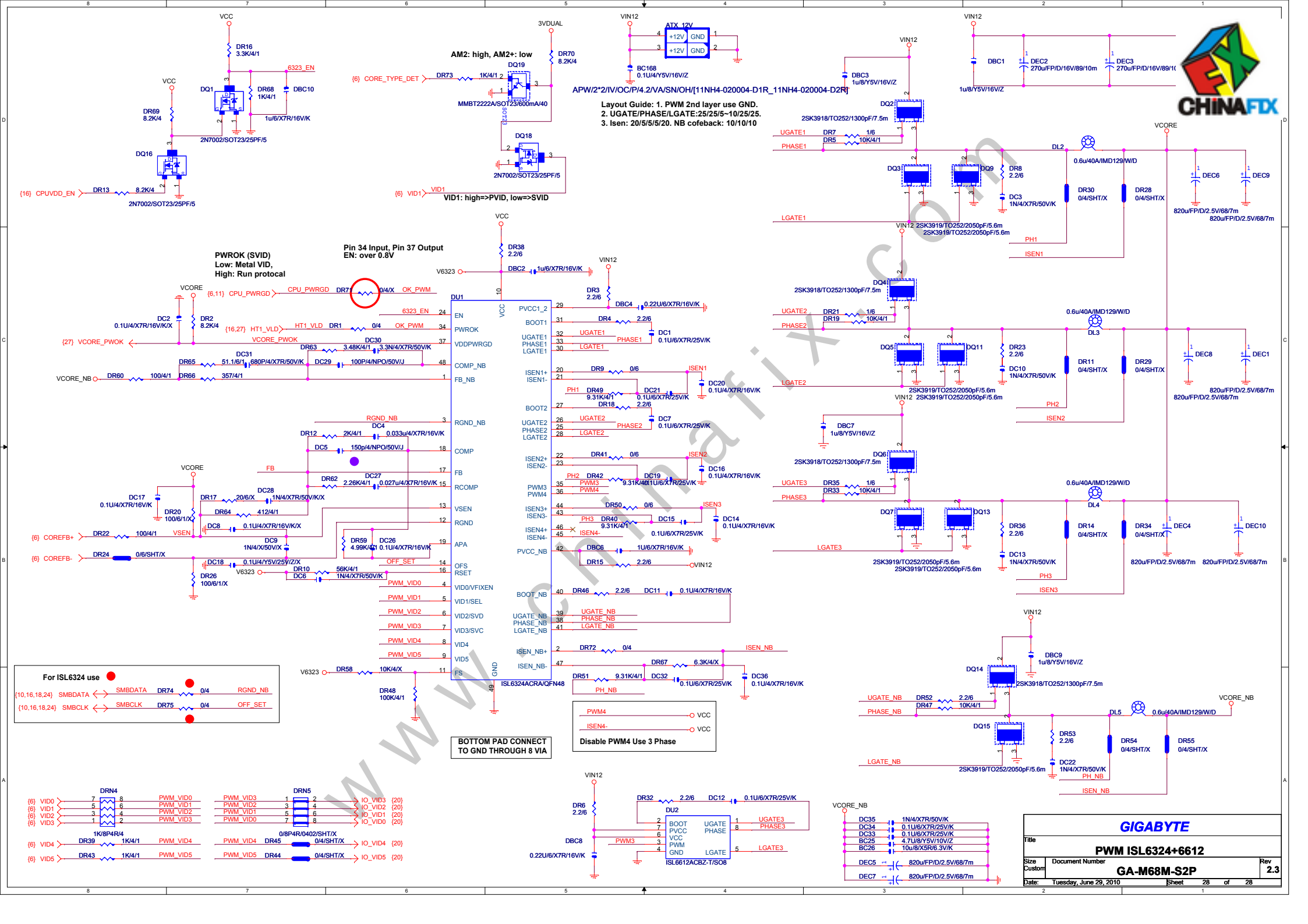
AM2: high, AM2+: low
VID1: high=>PVID, low=>SVID
PWROK (SVID)
Low: Metal VID,
High: Run protocal
Pin 34 Input, Pin 37 Output
EN: over 0.8V
APW/2*2/IV/OC/P/4.2/VA/SN/OH/[11NH4-020004-D1R_11NH4-020004-D2R]
Layout Guide: 1. PWM 2nd layer use GND.
2. UGATE/PHASE/LGATE:25/25/5~10/25/25.
3. Isen: 20/5/5/5/20. NB cofeback: 10/10/10
For ISL6324 use
Disable PWM4 Use 3 Phase
BOTTOM PAD CONNECT
TO GND THROUGH 8 VIA
ISL6324ACRA/QFN48
ISL6612ACBZ-T/SO8
2SK3918/TO252/1300pF/7.5m
2SK3919/TO252/2050pF/5.6m
GIGABYTE
PWM ISL6324+6612
GA-M68M-S2P
Tuesday, June 29, 2010